

- Fully programmable logic for signal processing and routing
- Inputs: External clock (single-ended or differential LVPECL), STAR TCD
- Outputs: External clock (differential LVPECL), Sync output
- Control/communication: 2x independent MCU-controlled CANbus interfaces
- Daughter card connection compatible with DDL-SIU fiber card format. Custom daughter cards may be used for specific applications
- 4x bi-directional interface to detector electronics

Pricing:

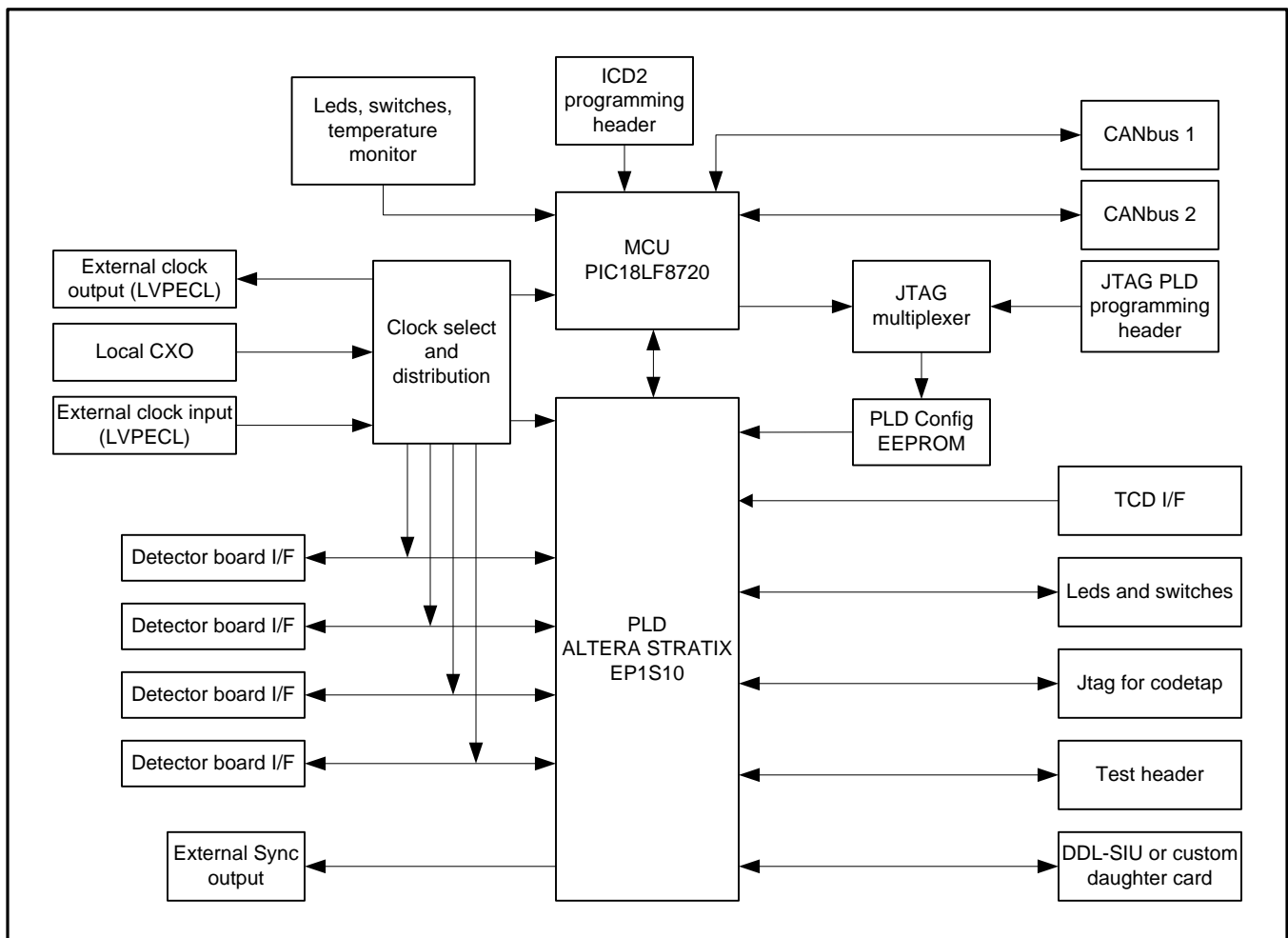
Quantity 1 – 4: \$3500 each

Quantity 5 – 9: \$3200 each

Quantity 10 – 99: \$3000

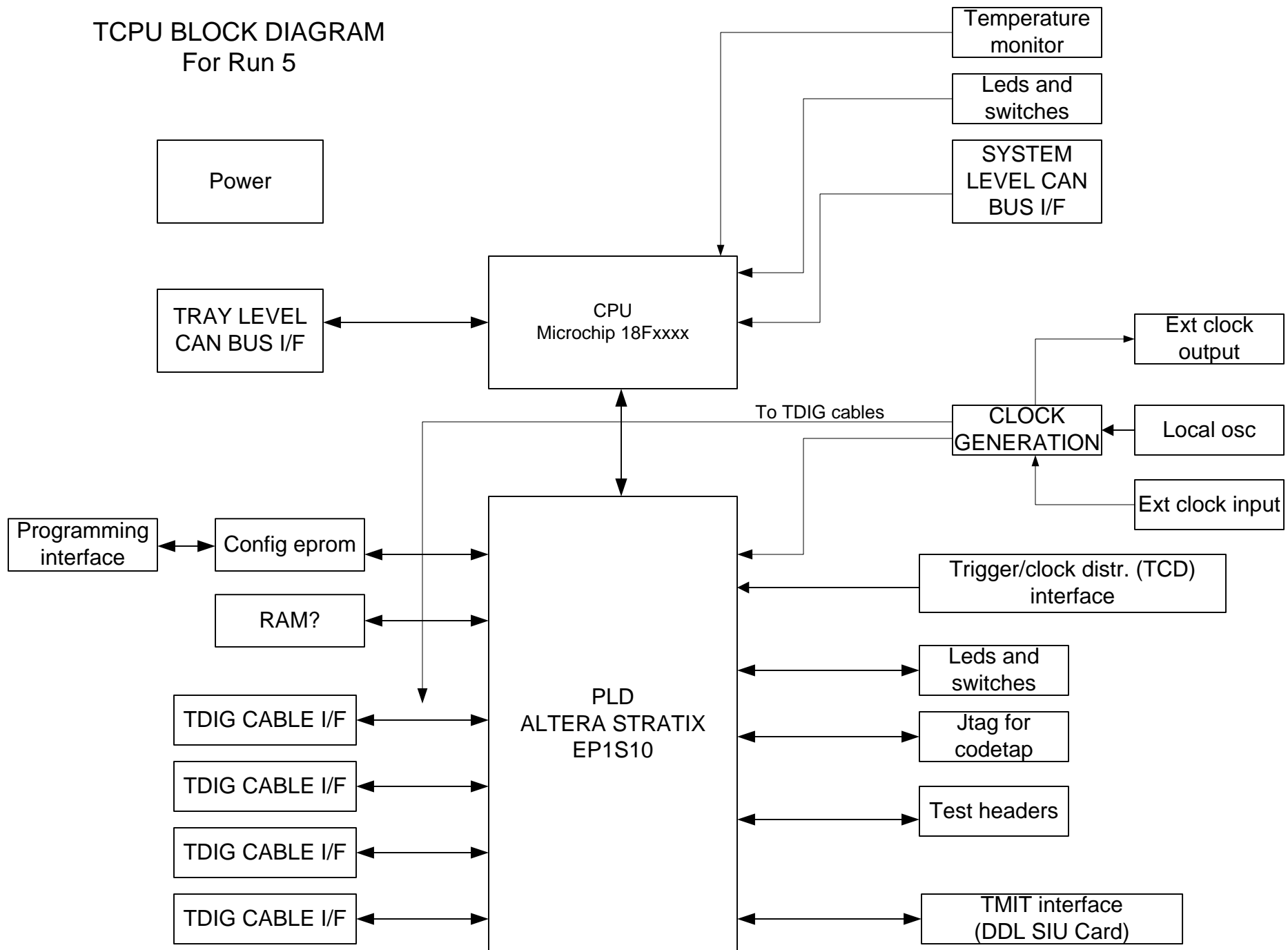
Quantity 100+: call for quote

(Prices are FOB Houston, TX)



TCPU block diagram

TCPU BLOCK DIAGRAM For Run 5



I've attached a block diagram that's almost current (there is no external RAM, but there's at least 1 Mbit inside the PLD.)

Each of the 4 ribbon cables has :

- 11 pairs of lvds input
- 4 pairs of lvds output
- 1 ttl wire in
- 1 ttl wire out
- 2 independent rs232 rs/tx pairs

The lvds driver/recievers are Texas Instruments 65lvds391 / 65lvds390. We're using them at 40 Mhz but they can go much faster, and the programmable logic chip can handle the higher rates.

I can give you more detail on the clock tree circuitry if that's an issue, but basically the board can receive, regenerate, and transmit the system clock to other tcpu boards and to the ribbon cables.

If you have any questions, don't hesitate to call, I'm sure I can help a little with your architecture.

Lloyd Bridges
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